What is claimed is:

1. A fuse and latch circuit comprising:
   a fuse having either a programmed state or an erased state;
   a latch that stores one of the programmed state or the erased state;
   a fuse read circuit coupled to the fuse and a reset indication signal, the fuse read circuit sensing the state of the fuse; and
   a transfer circuit, coupled between the fuse read circuit and the latch, for isolating the latch in response to a read operation caused by the reset indication signal such that the state stored in the latch remains after the reset indication signal indicates completion of the read operation.

2. The circuit of claim 1 and further including a clear circuit coupled to the latch for putting the latch into a predetermined state.

3. The circuit of claim 2 wherein the predetermined state is an erased state corresponding to a logical high.

4. The circuit of claim 1 wherein the programmed state is a logical low state and the erase state is a logical high state.

5. The circuit of claim 1 and further including an inverter coupling the fuse read circuit to the transfer circuit.

6. The circuit of claim 2 wherein the reset circuit is an n-channel transistor that is turned on by a fuse clear signal.

7. The circuit of claim 1 wherein the fuse read circuit comprises a p-channel transistor whose drive current, by applying a predetermined voltage to its gate, is reduced to allow a correct reading of the fuse.

8. The circuit of claim 1 wherein the fuse is a Floating gate Avalanche injection Metal Oxide Semiconductor transistor.

9. A no-precharge flash cell and latch circuit comprising:
a flash cell having either a programmed state or an erased state;
a latch circuit that stores one of the programmed state or the erased state from the flash cell;
a flash cell read circuit coupled to the flash cell and a reset indication signal, the flash cell read circuit sensing the state of the flash cell; and
a transmission gate, coupled between the flash cell read circuit and the latch circuit, for isolating the latch circuit when the reset indication signal is inactive and allowing the state of the flash cell through to the latch circuit when the reset indication signal is active.

10. The circuit of claim 9 wherein the latch circuit comprises a plurality of transistors organized to store a loaded state.

11. The circuit of claim 9 wherein the flash cell read circuit comprises a p-channel transistor as a pull up transistor whose drive current, by applying a predetermined voltage to its gate, is reduced to allow a correct reading of the flash cell, coupled to an n-channel transistor that is turned on by the reset indication signal.

12. The circuit of claim 9 wherein the transmission gate is further controlled by an inverse of the reset indication signal.

13. A flash cell and latch circuit comprising:
a flash cell having either a programmed state or an erased state that is read in response to an active wordline signal;

a latch circuit that stores one of the programmed state or the erased state from the flash cell;

a flash cell read circuit comprising a p-channel pull up transistor whose drive current, by applying a predetermined voltage to its gate, is reduced to allow a correct reading of the flash cell, coupled to an n-channel transistor that is turned on by a reset indication signal such that a node between the p-channel and n-channel transistors is pulled up to a logical high state when the wordline signal is active, the flash cell state is programmed, and the n-channel transistor is turned on;

an inverter coupled to the node to invert the logical high state to a logical low state; and

a transmission gate, coupled between the inverter and the latch circuit, for isolating the latch circuit when the reset indication signal is inactive and allowing the logical low state through to the latch circuit when the reset indication signal is active.

14. The circuit of claim 13 wherein the node is at a logical low state when the wordline is active, the flash cell state is erased, and the n-channel transistor is turned on such that the transmission gate allows a resulting logical high state from the inverter through to the latch circuit when the reset indication signal is active.

15. The circuit of claim 13 and further including a clearing transistor coupled to the latch circuit to reset the latch circuit to a known state.

16. A flash cell and latch circuit comprising:

a flash cell having either a programmed state or an erased state that is read in response to an active wordline signal;

a latch circuit that stores one of the programmed state or the erased state from the flash cell;

a flash cell read circuit comprising a p-channel pull up transistor whose drive current, by applying a predetermined voltage to its gate, is reduced to allow a correct reading of the flash cell, coupled to an n-channel transistor that is turned on by a reset indication signal such that a node between the p-channel and n-channel transistors is pulled up to a logical high state when the wordline signal is active, the flash cell state is programmed, and the n-channel transistor is turned on;

a logic control circuit coupled to the node and the reset indication signal, the logic control circuit generating a programmed state control signal and an erased state control signal in response to voltage level of the node and the reset indication signal;

a first control transistor, coupled to the programmed state control signal, that puts the latch circuit into the programmed state when the programmed state control signal is active; and

a second control transistor, coupled to the erased state control signal, that puts the latch circuit into the erased state when the erased state control signal is active.

17. The circuit of claim 16 wherein the logic control circuit comprises:

a NAND gate having a first input coupled to the node and a second input coupled to the reset indication signal, the NAND gate generating the programmed state control signal;

an inverter gate having an input coupled to the reset indication signal and generating an inverse reset indication signal; and

a NOR gate having a first input coupled to the node and a second input coupled to the inverse reset indication signal, the NOR gate generating the erased state control signal.

18. A method for latching a fuse state, in a memory device, that does not require a precharge after a reset condition, the method comprising:

reading the fuse state;

if the fuse state is in a programmed state, storing a logic low state through a transmission gate into a latch circuit;

resetting the memory device; and

reading the logic low state from the latch circuit without precharging the latch circuit from the fuse.

19. A method for latching a state of a Floating gate Avalanche injection Metal Oxide Semiconductor cell into a latch circuit in a memory device, the method comprising:

reading a state of the cell;

latching the state into the latch circuit;

isolating the latch circuit from the cell;

resetting at least a portion of the memory device; and

reading the state from the latch circuit without precharging the latch circuit from the cell.

20. An electronic system comprising:

a processor that generates control signals; and

a memory device, coupled to the processor, that operates in response to the control signals, the memory device having a fuse and latch circuit that does not require a precharge operation after a reset condition, the circuit comprising:

a fuse having either a programmed state or an erased state;

a latch that stores one of the programmed state or the erased state;

a fuse read circuit coupled to the fuse and a reset indication signal, the fuse read circuit sensing the state of the fuse; and

a transfer circuit, coupled between the fuse read circuit and the latch, for isolating the latch in response to the reset indication signal such that the state stored in the latch remains after the reset indication signal indicates completion of a reset operation.

21. The electronic system of claim 20 wherein the memory device is a NAND-type memory device.

22. The electronic system of claim 21 wherein the memory device is a NOR-type memory device.